Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 71709

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2017.

Seventh Semester

Electronics and Communication Engineering

EC 6009 — ADVANCED COMPUTER ARCHITECTURE

(Regulations 2013)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define spatial and temporal locality.

2. What is dependability?

3. List the major advantages of dynamic scheduling using Tomasulo's approach.

4. What is data hazard?

5. What are the omissions in the SIMD extension instruction set?

6. Describe the similarities and differences between Multimedia SIMD computers and GPU.

7. What is multicore architecture?

8. What is the major disadvantage of DSM architecture?

9. What the similarities and differences between SCSI and IDE?

10. Explain the need to implement memory as a hierarchy.

PART B — (5 × 16 = 80 marks)

11. (a) Explain in detail about trends in power and energy in integrated circuits with suitable example. (16)

Or

(b) (i) Suppose we have made the following measurements :

Frequency of FP operations = 25%

Average CPI of FP operations = 4.0

Avenge CPI of other instructions = 1.33

Frequency of FPSQR = 2%

CPI of FPSQR = 20

Assume that the two design alternatives are to decrease the CPI of FPSQR to 2 or to decrease the average CPI of all FP operations to 2.5. Compare these two design alternatives using the processor performance equation. (6)

(ii) Discuss about the guidelines and principles that are useful in design and evaluate the performance of computer systems with example. (10)

12. (a) (i) Describe the basic compiler techniques for exploiting instruction level parallelism. (10)

(ii) Briefly compare the hardware and software speculation. (6)

Or

(b) (i) Explain the methods of exploiting LIP using VLIW processor. (8)

(ii) Discuss the important limitations to ILP. (8)

13. (a) Explain Data level parallelism in Vector architecture in detail. (16)

Or

(b) Discuss GPU architecture with neat diagram. (16)

14. (a) With neat diagram, explain the distributed shared memory architecture. (16)

(b) (i) Explain about synchronization techniques used in multiprocessor system. (10)

(ii) Discuss about models of memory consistency. (6)

15. (a) Describe various basic cache optimization techniques with example. (16)

Or

(b) (i) Briefly describe about various RAID levels with diagram. (8)

(ii) List and explain various I/O performance measures. (8)